# AOC-400G-Q56DD-200G
## 2Q56-5MSKY

Dell AOC-400G-Q56DD-200G 2Q56-5M Compatible 400GBase-AOC QSFP-DD to 2xQSFP56 Active Optical Cable (850nm, MMF, 5m)

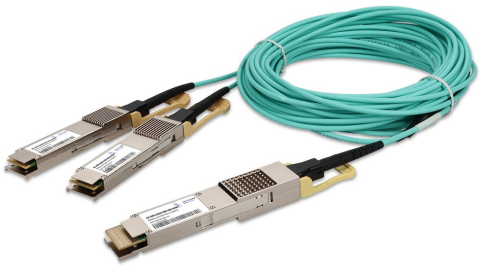
**Product Description**

This is an Dell® AOC-400G-Q56DD-200G 2Q56-5M (16.4ft) compatible 400GBase QSFP-DD 400G to 2xQSFP56 200G active optical cable that operates over multi-mode fiber with a maximum reach of 5.0m. At a wavelength of 850nm, it has been programmed, uniquely serialized, and data-traffic and application tested to ensure it is 100% compliant and functional. This active optical cable is built to comply with MSA (Multi-Source Agreement) standards. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

Skylane's transceivers are RoHS compliant and lead-free.

**Features:**

- Supports 26.5625GBd PAM4 and 25.78125Gbps NRZx4 Channels Per Cable
- 850nm VCSEL and PIN Receiver
- OM3 MMF
- Hot Pluggable
- Single 3.3V Power Supply
- QSFP-DD and QSFP56 MSA Package
- Operating Temperature Range: 0 to 70 Celsius
- Maximum Power Consumption of 8.5W on QSFP-DD End and 5W on Each QSFP56 End
- RoHS Compliant and Lead-Free



**Applications:**

- 400GBase Ethernet

*For your product safety, please read the following information carefully before any manipulation of the transceiver:*

*ESD*
*This transceiver is specified as ESD threshold 1kV for SFI pins and 2kV for all others electrical input pins, tested per MIL-STD-883G, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module.*

*LASER SAFETY*
*This is a Class1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).*

***The optical ports of the module need to be terminated with an optical connector or with a dust plug in order to avoid contamination.***

## General Specifications

| Parameter | | Symbol | Min | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Storage Temperature** | | Tstg | -40 | | 85 | °C |
| **Operating Case Temperature** | | Tc | 0 | | 70 | °C |
| **Supply Voltage** | | Vcc | 0 | | 3.63 | V |
| **Operating Humidity (Non-Condensing)** | | | 5 | | 85 | % |
| **Supply Current** | **QSFP-DD** | Icc | | | 2575 | |
| | **QSFP56** | Icc | | | 1450 | |
| **Module Power Dissipation** | **QSFP-DD** | P | | | 8.5 | |
| | **QSFP56** | P | | | 5 | |
| **Power Supply Voltage** | | Vcc | 3.135 | 3.3 | 3.465 | V |

## QSFP-DD I/O Timing Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **MgmtInit Duration** | Max. MgmtInit Duration | | | 2000 | ms | 1 |
| **ResetL Assert Time** | t_reset_init | 10 | | | µs | 2 |
| **IntL Assert Time** | ton_IntL | | | 200 | ms | 3 |
| **IntL De-Assert Time** | toff_IntL | | | 500 | µs | 4 |
| **Rx_LOS Assert Time** | ton_los | | | 100 | ms | 5 |
| **Flag Assert Time** | ton_flag | | | 200 | ms | 6 |
| **Mask Assert Time** | ton_mask | | | 100 | ms | 7 |
| **Mask De-Assert Time** | toff_mask | | | 100 | ms | 8 |

**Notes:**

1. Time from power on, hot plug, or rising edge of reset until the completion of the MgmtInit state.
2. Minimum pulse time on the ResetL signal to initiate a module reset.
3. Time from occurrence of condition triggering IntL until VOUT: IntL=VOL.
4. Time from clear on read operation of associated flag until VOUT: IntL=VOH. This includes de-assert times for Rx_LOS, Tx_Fault, and other flag bits.
5. Time from Rx_LOS state to Rx_LOS bit is set (value = 1b), and the IntL is asserted.
6. Time from occurrence of condition triggering flag to associated flag bit is set (value = 1b), and the IntL is asserted.
7. Time from mask bit is set (value = 1b) until the associated IntL assertion is inhibited.
8. Time from mask bit is cleared (value = 0b) until the associated IntL operation resumes.

**QSFP56 I/O Timing Characteristics**

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **Initialization Time** | t_init | | | 2 | s | 1 |
| **Reset Init Assert Time** | t_reset_init | 10 | | | µs | 2 |
| **Serial Bus Hardware Ready Time** | t_serial | | | 2 | s | 3 |
| **Monitor Data Ready Time** | t_data | | | 2 | s | 4 |
| **Reset Assert Time** | t_reset | | | 2 | s | 5 |
| **LPMode/TxDis Mode Change Time** | t_LPMode/TxDis | | | 100 | ms | 6 |
| **LPMode Assert Time** | ton_LPMode | | | 100 | ms | 7 |
| **LPMode De-Assert Time** | toff_LPMode | | | 300 | ms | 8 |
| **IntL/RxLOSL Mode Change Time** | t_IntL/RxLOSL | | | 100 | ms | 9 |
| **IntL Assert Time** | ton_IntL | | | 200 | ms | 10 |
| **IntL De-Assert Time** | toff_IntL | | | 500 | µs | 11 |
| **Rx_LOS Assert Time** | ton_LOS | | | 100 | ms | 12 |
| **Tx_Fault Assert Time** | ton_Txfault | | | 200 | ms | 13 |
| **Flag Assert Time** | ton_flag | | | 200 | ms | 14 |
| **Mask Assert Time** | ton_mask | | | 100 | ms | 15 |
| **Mask De-Assert Time** | toff_mask | | | 100 | ms | 16 |
| **Power Override or Power-Set Assert Time** | ton_Pdown | | | 100 | ms | 17 |
| **Power Override or Power-Set De-Assert Time** | toff_Pdown | | | 300 | ms | 18 |

**Notes:**

1. Time from power on, or hot plug, until the module is fully functional. This time applies to Power Class 2 or higher modules when LPMode is pulled “low” by the host and to all Power Class 1 modules.
2. Host is required to provide a reset pulse of at least the minimum value for the module to guarantee a reset sequence. Shorter pulses may reset the module depending on implementation.
3. Time from power on until the module responds to data transmission over the 2-wire serial bus.
4. Time from power on to “Data Not Ready,” Byte 2 Bit 0, cleared to 0 and IntL output is pulled “low.”
5. Time from a rising edge on the ResetL input until the module is fully functional.
6. Time to change between LPMode and TxDis modes of the dual mode signal LPMode/TxDis.
7. Time from when the host releases LPMode to “high” until the module’s power consumption reaches Power Class 1.
8. Time from when the host pulls LPMode “low” until the module is fully functional.
9. Time to change between IntL and RxLOSL modes of the dual mode signal IntL/RxLOSL.
10. Time from the occurrence of condition triggering an interrupt until IntL is “low.”
11. Time from clear on read operation of associated flag until module releases IntL to “high.” This includes the time to clear Rx_LOS, Tx_Fault, and other flag bits.
12. Time from Rx optical signal loss to Rx_LOS bit is set to 1, and the IntL is pulled “low” by the module.

13. Time from Tx_Fault state to Tx_Fault bit is set to 1, and the IntL is pulled “low” by the module.
14. Time from condition triggering flag to associated flag bit is set to 1, and the IntL is pulled “low” by the module.
15. Time from mask bit is set to 1 until the module is prevented from pulling the IntL “low” when the associated flag is set “high.”
16. Time from mask bit is cleared to 0 until the module is enabled to pull the IntL “low” when the associated flag is set “high.”
17. Time from Power_Override or Power_Set bit is set to 1 until the module’s power consumption reaches Power Class 1.
18. Time from Power_Override or Power_Set bit is cleared to 0 until the module is fully functional.

**Optical Characteristics**

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **Transmitter** | | | | | | |
| **Data Rate Per Lane** | DR | | 26.5625 | | GBd | |
| **Modulation Format** | MF | | PAM4 | | | |
| **Signaling Speed Accuracy** | SSA | -100 | | 100 | ppm | |
| **Center Wavelength** | CW | | 850 | | nm | |
| **RMS Spectral Width** | Δλ | | | 0.6 | nm | |
| **Average Optical Power** | PO | -6.5 | | 4 | dBm | |
| **Laser Off Power** | Poff | | | -30 | dBm | |
| **Receiver** | | | | | | |
| **Data Rate Per Lane** | DR | | 26.5625 | | GBd | |
| **Modulation Format** | MF | | PAM4 | | | |
| **Differential Data Output Voltage Pk-Pk Swing** | Vopp | | | 900 | mV | |
| **Differential Output Impedance** | Zos | 90 | 100 | 110 | Ω | |
| **Common-Mode Voltage** | Vcm | -350 | | 2850 | mV | |
| **Common-Mode Noise RMS** | | | | 17.5 | mV | |
| **Differential Output Return Loss** | SDD22 | OIF CEI-56G-VSR-PAM4 and 400GAUI-8 Requirements | | | dB | |
| **Common-Mode to Differential Conversion and Differential to Common-Mode Conversion** | SDC22<br>SCD22 | | | | | |
| **Common-Mode Return Loss** | SCC22 | | | -2 | dB | |

## QSFP-DD Pin Descriptions

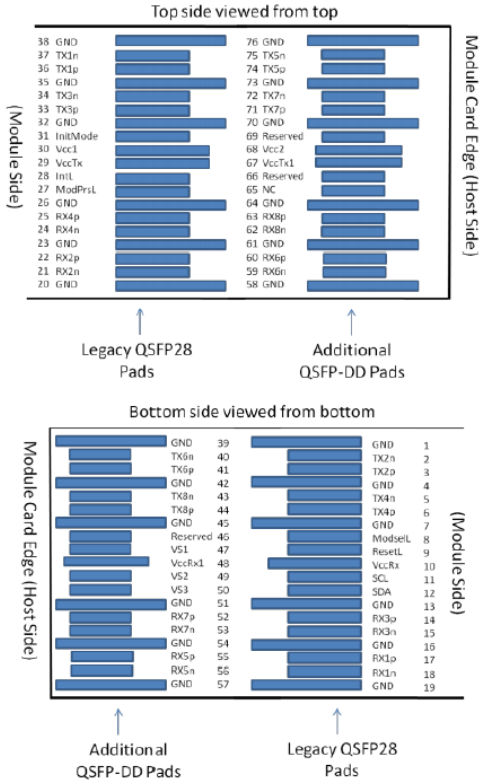
| Pin | Logic | Symbol | Name/Description | Plug Sequence | Notes |
|---|---|---|---|---|---|
| **1** | | GND | Module Ground. | 1B | 1 |
| **2** | CML-I | Tx2- | Transmitter Inverted Data Input. | 3B | |
| **3** | CML-I | Tx2+ | Transmitter Non-Inverted Data Input. | 3B | |
| **4** | | GND | Module Ground. | 1B | 1 |
| **5** | CML-I | Tx4- | Transmitter Inverted Data Input. | 3B | |
| **6** | CML-I | Tx4+ | Transmitter Non-Inverted Data Input. | 3B | |
| **7** | | GND | Module Ground. | 1B | 1 |
| **8** | LVTTL-I | ModSelL | Module Select. | 3B | |
| **9** | LVTTL-I | ResetL | Module Reset. | 3B | |
| **10** | | VccRx | +3.3V Receiver Power Supply. | 2B | 2 |
| **11** | LVCMOS–I/O | SCL | 2–Wire Serial Interface Clock. | 3B | |
| **12** | LVCMOS–I/O | SDA | 2–Wire Serial Interface Data. | 3B | |
| **13** | | GND | Module Ground. | 1B | 1 |
| **14** | CML-O | Rx3- | Transmitter Inverted Data Output. | 3B | |
| **15** | CML-O | Rx3+ | Transmitter Non-Inverted Data Output. | 3B | |
| **16** | | GND | Module Ground. | 1B | 1 |
| **17** | CML-O | Rx1- | Transmitter Inverted Data Output. | 3B | |
| **18** | CML-O | Rx1+ | Transmitter Non-Inverted Data Output. | 3B | |
| **19** | | GND | Module Ground. | 1B | 1 |
| **20** | | GND | Module Ground. | 1B | 1 |
| **21** | CML-O | Rx2- | Transmitter Inverted Data Output. | 3B | |
| **22** | CML-O | Rx2+ | Transmitter Non-Inverted Data Output. | 3B | |
| **23** | | GND | Module Ground. | 1B | 1 |
| **24** | CML-O | Rx4- | Transmitter Inverted Data Output. | 3B | |
| **25** | CML-O | Rx4+ | Transmitter Non-Inverted Data Output. | 3B | |
| **26** | | GND | Module Ground. | 1B | 1 |
| **27** | LVTTL-O | ModPrsL | Module Present. | 3B | |
| **28** | LVTTL-O | IntL | Interrupt. | 3B | |
| **29** | | VccTx | +3.3V Transmitter Power Supply. | 2B | 2 |
| **30** | | Vcc1 | +3.3V Power Supply. | 2B | 2 |
| **31** | LVTTL-I | InitMode | Initialization Mode. In legacy QSFP applications, the InitMode pad is called LPMODE. | 3B | |
| **32** | | GND | Module Ground. | 1B | 1 |
| **33** | CML-I | Tx1- | Transmitter Inverted Data Input. | 3B | |
| **34** | CML-I | Tx1+ | Transmitter Non-Inverted Data Input. | 3B | |
| **35** | | GND | Module Ground. | 1B | 1 |

| | | | | | |
|---|---|---|---|---|---|
| **36** | CML-I | Tx1- | Transmitter Inverted Data Input. | 3B | |
| **37** | CML-I | Tx1+ | Transmitter Non-Inverted Data Input. | 3B | |
| **38** | | GND | Module Ground. | 1B | 1 |
| **39** | | GND | Module Ground. | 1A | 1 |
| **40** | CML-I | Tx6- | Transmitter Inverted Data Input. | 3A | |
| **41** | CML-I | Tx6+ | Transmitter Non-Inverted Data Input. | 3A | |
| **42** | | GND | Module Ground. | 1A | 1 |
| **43** | CML-I | Tx8- | Transmitter Inverted Data Input. | 3A | |
| **44** | CML-I | Tx8+ | Transmitter Non-Inverted Data Input. | 3A | |
| **45** | | GND | Module Ground. | 1A | 1 |
| **46** | | Reserved | Not Connected. | 3A | 3 |
| **47** | | VS1 | Not Connected. | 3A | 3 |
| **48** | | VccRx1 | + 3.3V Receiver Power Supply. | 2A | 2 |
| **49** | | VS2 | Not Connected. | 3A | 3 |
| **50** | | VS3 | Not Connected. | 3A | 3 |
| **51** | | GND | Module Ground. | 1A | 1 |
| **52** | CML-O | Rx7- | Transmitter Inverted Data Output. | 3A | |
| **53** | CML-O | Rx7+ | Transmitter Non-Inverted Data Output. | 3A | |
| **54** | | GND | Module Ground. | 1A | 1 |
| **55** | CML-O | Rx5- | Transmitter Inverted Data Output. | 3A | |
| **56** | CML-O | Rx5+ | Transmitter Non-Inverted Data Output. | 3A | |
| **57** | | GND | Module Ground. | 1A | 1 |
| **58** | | GND | Module Ground. | 1A | 1 |
| **59** | CML-O | Rx6- | Transmitter Inverted Data Output. | 3A | |
| **60** | CML-O | Rx6+ | Transmitter Non-Inverted Data Output. | 3A | |
| **61** | | GND | Module Ground. | 1A | 1 |
| **62** | CML-O | Rx8- | Transmitter Inverted Data Output. | 3A | |
| **63** | CML-O | Rx8+ | Transmitter Non-Inverted Data Output. | 3A | |
| **64** | | GND | Module Ground. | 1A | 1 |
| **65** | | NC | Not Connected. | 3A | 3 |
| **66** | | Reserved | Not Connected. | 3A | 3 |
| **67** | | VccTx1 | +3.3V Transmitter Power Supply. | 2A | 2 |
| **68** | | Vcc2 | +3.3V Power Supply. | 2A | 2 |
| **69** | | Reserved | Not Connected. | 3A | 3 |
| **70** | | GND | Module Ground. | 1A | 1 |
| **71** | CML-I | Tx7- | Transmitter Inverted Data Input. | 3A | |
| **72** | CML-I | Tx7+ | Transmitter Non-Inverted Data Input. | 3A | |

| | | | | | |
|---|---|---|---|---|---|
| **73** | | GND | Module Ground. | 1A | 1 |
| **74** | CML-I | Tx5- | Transmitter Inverted Data Input. | 3A | |
| **75** | CML-I | Tx5+ | Transmitter Non-Inverted Data Input. | 3A | |
| **76** | | GND | Module Ground. | 1A | 1 |

**Notes:**

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module, and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane. This pin is an open collector/drain output pin and shall be pulled up with 4.7kΩ to 10kΩ to the Host_Vcc on the host board. Pull-ups can be connected to multiple power supplies; however, the host board design shall ensure that no module pin has a voltage exceeding the module VccT/R+0.5V.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx, and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed below. VccRx, VccRx1, Vcc1, Vcc2, VccTx, and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000mA.
3. All Vendor-Specific, Reserved, and Not Connected pins may be terminated with 50Ω to the ground on the host. Pad 65 (Not Connected) shall be left unconnected within the module. Vendor-Specific and Reserved pads shall have an impedance to the GND that is greater than 10kΩ and less than 100pF.
4. Plug Sequence specifies the mating sequence of the host connector and the module. The sequence is 1A, 2A, 3A, 1B, 2B, and 3B. See below for pad locations. Contact Sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.



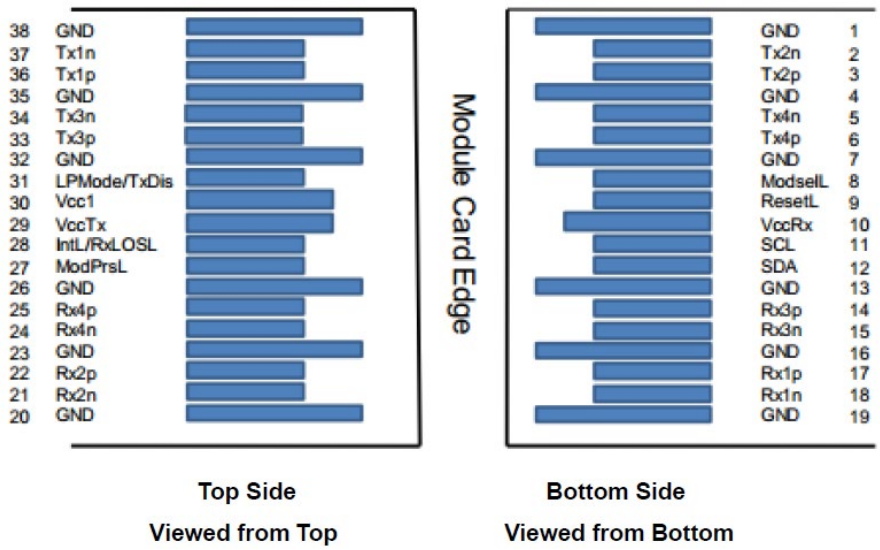
## QSF56 Pin Descriptions

| Pin | Symbol | Name/Description | Notes |
|---|---|---|---|
| **1** | GND | Module Ground. | 1 |
| **2** | Tx2- | Transmitter Inverted Data Input. | |
| **3** | Tx2+ | Transmitter Non-Inverted Data Input. | |
| **4** | GND | Module Ground. | 1 |
| **5** | Tx4- | Transmitter Inverted Data Input. | |
| **6** | Tx4+ | Transmitter Non-Inverted Data Input. | |
| **7** | GND | Module Ground. | |
| **8** | ModSelL | Module Select. | |
| **9** | ResetL | Module Reset. | |
| **10** | VccRx | +3.3V Receiver Power Supply. | 2 |
| **11** | SCL | 2-Wire Serial Interface Clock. | |
| **12** | SDA | 2-Wire Serial Interface Data. | |
| **13** | GND | Module Ground. | |
| **14** | Rx3+ | Receiver Non-Inverted Data Output. | |
| **15** | Rx3- | Receiver Inverted Data Output. | |
| **16** | GND | Module Ground. | 1 |
| **17** | Rx1+ | Receiver Non-Inverted Data Output. | |
| **18** | Rx1- | Receiver Inverted Data Output. | 1 |
| **19** | GND | Module Ground. | 1 |
| **20** | GND | Module Ground. | |
| **21** | Rx2- | Receiver Inverted Data Output. | |
| **22** | Rx2+ | Receiver Non-Inverted Data Output. | |
| **23** | GND | Module Ground. | |
| **24** | Rx4- | Receiver Inverted Data Output. | |
| **25** | Rx4+ | Receiver Non-Inverted Data Output. | |
| **26** | GND | Module Ground. | 1 |
| **27** | ModPrsL | Module Present. | |
| **28** | IntL/RxLOSL | Interrupt. Optionally configurable as RxLOSL via the management interface (SFF-8636). | |
| **29** | VccTx | +3.3V Transmitter Power Supply. | 2 |
| **30** | Vcc1 | +3.3V Power Supply. | 2 |
| **31** | LPMode/TxDis | Low-Power Mode. Optionally configurable as TxDis via the management interface (SFF-8636). | |
| **32** | GND | Module Ground. | 1 |
| **33** | Tx3+ | Transmitter Non-Inverted Data Input. | |
| **34** | Tx3- | Transmitter Inverted Data Input. | |
| **35** | GND | Module Ground. | 1 |

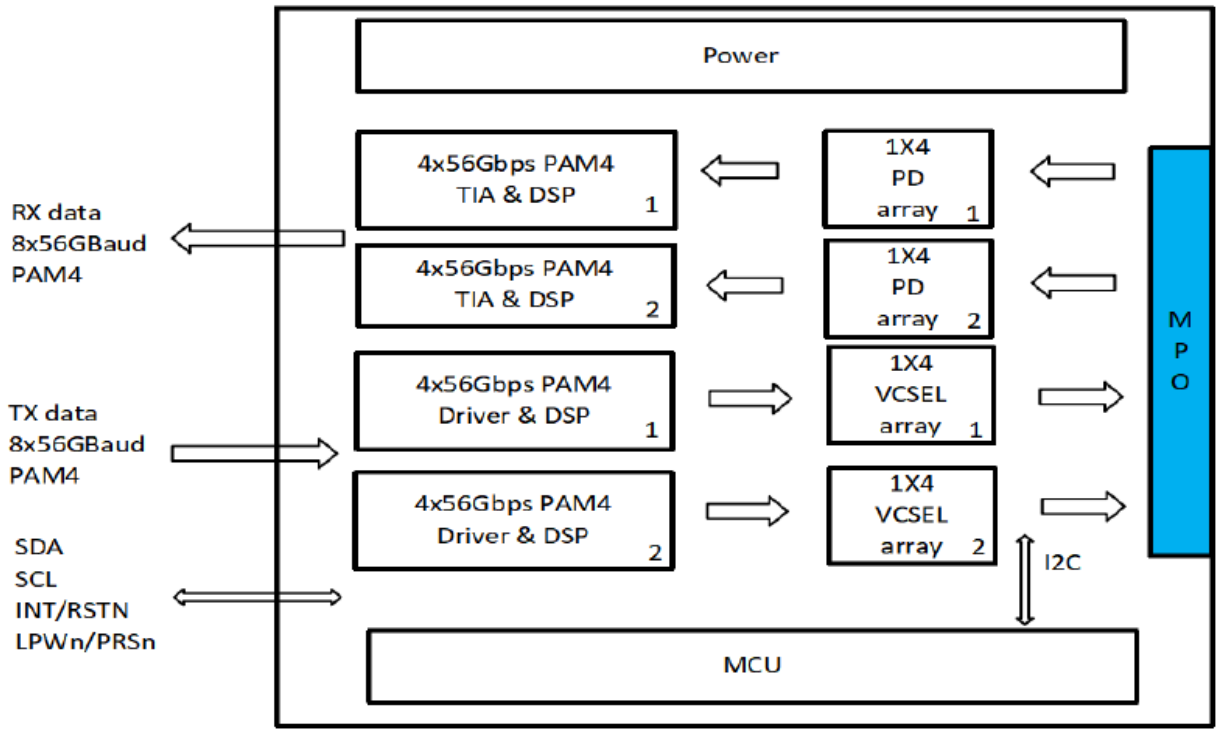
| | | | |
|---|---|---|---|
| **36** | Tx1+ | Transmitter Non-Inverted Data Input. | |
| **37** | Tx1- | Transmitter Inverted Data Input. | |
| **38** | GND | Module Ground. | 1 |

**Notes:**

1. GND is the symbol for signal and power supply common for the module. All are common within the module, and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, Vcc1, and VccTx are applied concurrently and may be internally connected within the module in any combination. Vcc contacts in SFF-8662 and SFF-8672 each have a steady state current rating of 1A.



**QSFP-DD Block Diagram of Transceiver**

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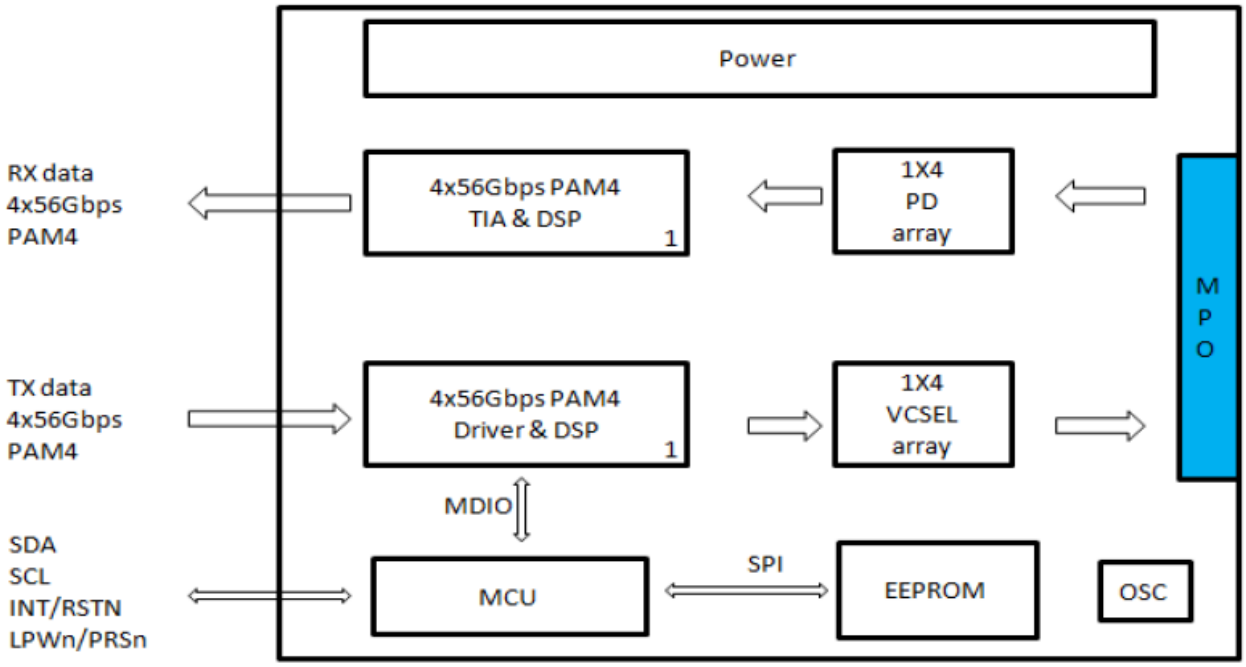
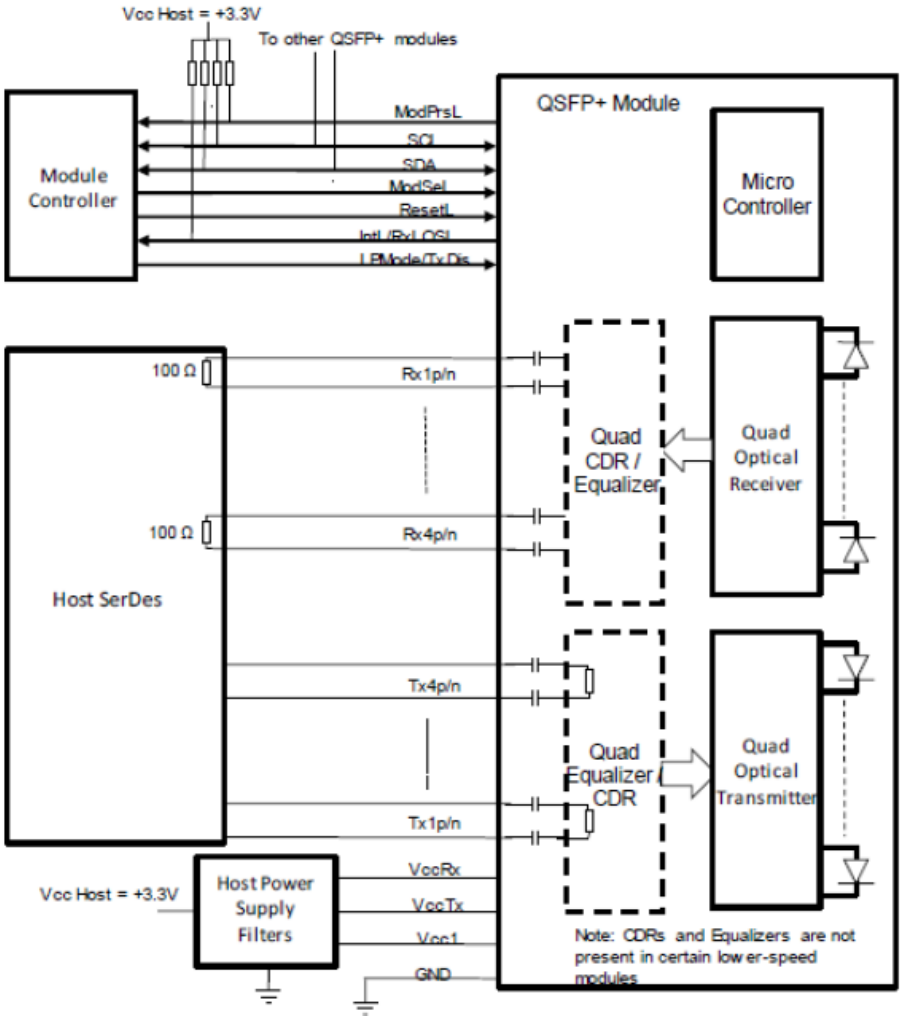
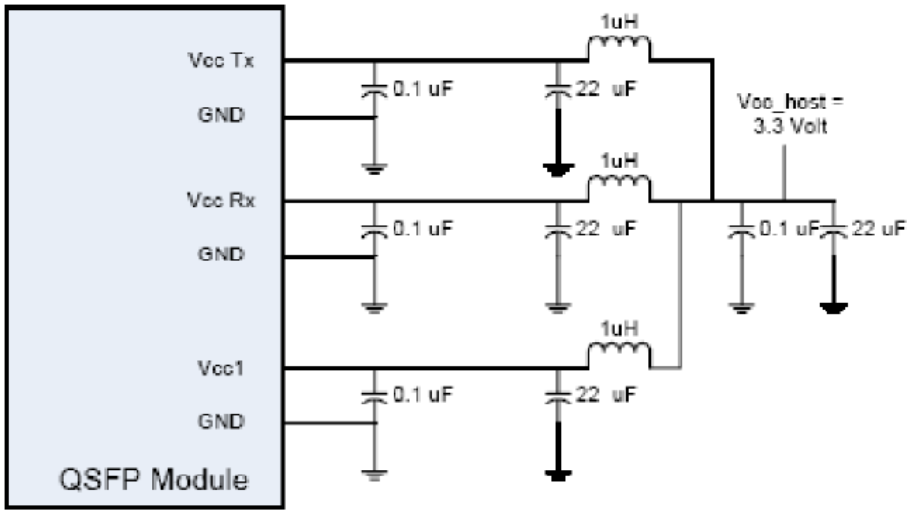


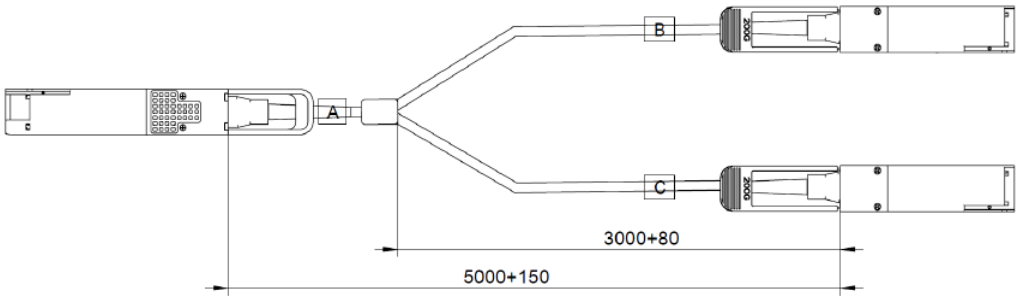
**QSFP-DD Host Board**



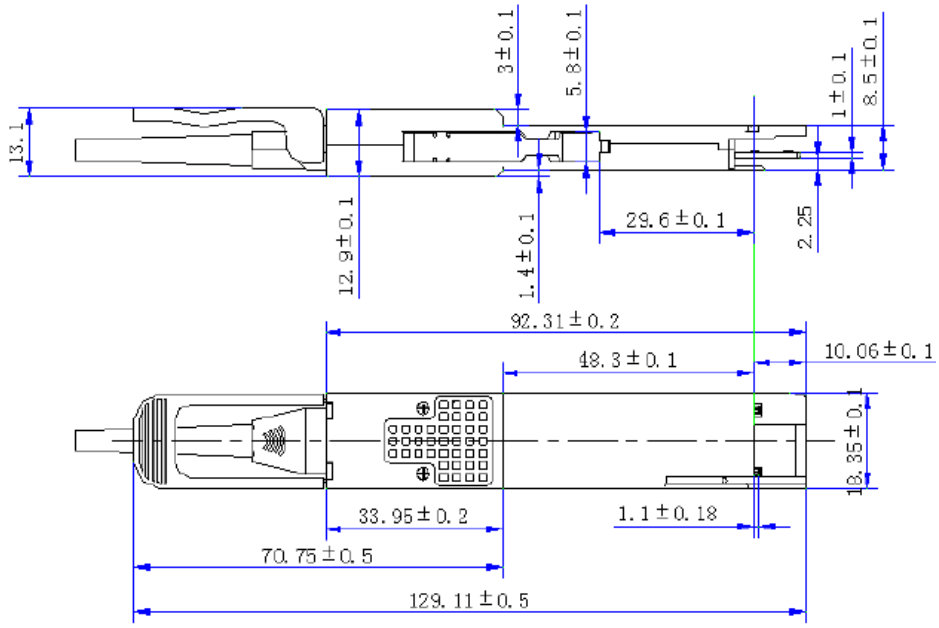

**QSFP56 Host Board**



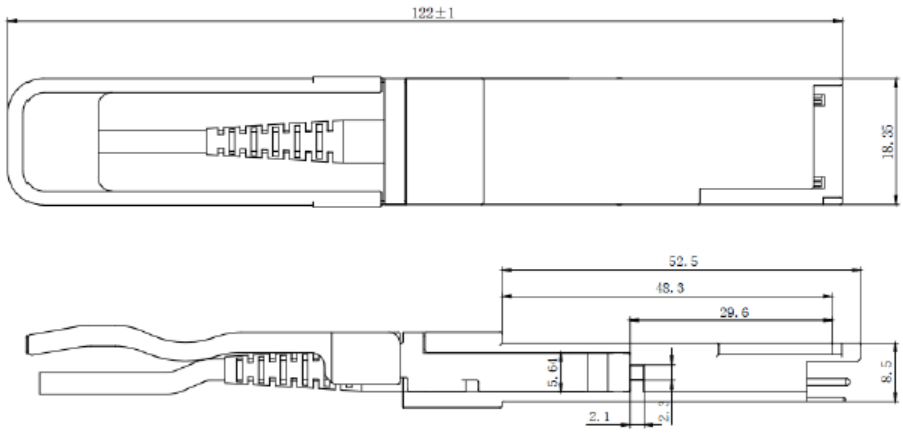
## Mechanical Specifications




## QSFP-DD Mechanical Specifications




## QSFP56 Mechanical Specifications



# About Skylane Optics

Skylane is a leading provider of transceivers for optical communication.

We offer an extensive portfolio for the enterprise, access, datacenter and metropolitan fiber optical market as well as for smart home applications and home networks.

We cover the European, South American and North American market with a strong partner network and have offices in Belgium, Brazil, Sweden and USA.

Our offerings are characterized by high quality and performance. In combination with our strong technical support, we enable our customers to build cost optimized network solutions.

We offer an extensive range of high-quality products including transceivers (Optical and copper), Active Optical Cable (AOC), Direct Attach Cable (DAC), Mux/Demux, Coding Box.